Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims:

1-20. (canceled).

21. (currently amended) A storage system comprising:

a plurality of disk drives configuring at least one logical volume;

a plurality of processor adapters each ~~including at least one processor and~~ controlling to store data, which are sent from at least one host computer to said at least one logical volume, in a plurality of said disk drives;

a plurality of first interface adapters each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer and sending a first control information related to said write request to at least one of said processor adapters and sending data received at each of said first interface adapters based on a second control information sent from said at least one processor adapter;

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapters;

a plurality of second interface adapters each coupled to said disk drives and receiving data stored in said cache memory adapter from said cache memory adapter based on a third control information sent from said at least one processor adapter asynchronously with receipt of said write request at said first interface

adapters and storing data received at each of said second interface adapters in said disk drives; and

a switch adapter coupled to said processor adapters, said first interface adapters, said cache memory adapter and said second interface adapters and relaying data between said first interface adapters and said cache memory adapter and relaying data between said cache memory adapter and said second interface adapters;

~~wherein said switch adapter relays said first and said second control information between said processor adapters and said first interface adapters and relays said third control information between said processor adapters and said second interface adapters.~~

wherein a number of said processor adapters is increased or decreased independently of the first and second interface adaptors, said cache memory adaptor and said switch adaptor, based on a required performance, ~~and~~

wherein all of said processor adapters can access to each of said first interface adapters and each of said second interface adapters, and

wherein each of said processor adapters ~~has~~includes a plurality of ~~micro~~processors and, when a first processing load at said first interface adapters which are coupled to said at least one host computer is greater than a second processing load at said second interface adapters which are coupled to said disk drives, the number of processors allocated to said first processing load at said first interface adapters is larger than the number of processors allocated to said second processing load at said second interface adapters, and

wherein when said second processing load of said second interface adapters is greater than said first processing load at said first interface adapters, the number of processors allocated to said second processing load of said second interface adapters is larger than the number of said first processing load of said first interface adapters~~each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapters or a second processing load sent from said second interface adapters in accordance with an amount of said first processing load and an amount of said second processing load~~.

22. (canceled).

23. (previously presented) The storage system according to claim 21 wherein:

said processor adapters are assigned to a process of at least one of said first interface adapters and a process of at least one of said second interface adapters.

24. (previously presented) The storage system according to claim 21 wherein:

said at least one processor adapter is assigned to said plurality of first interface adapters.

25. (previously presented) The storage system according to claim 21 wherein:

said at least one processor adapter is assigned to said plurality of second interface adapters.

26. (canceled).

27. (currently amended) The storage system according to claim 26 wherein:

it is possible to change the number of said processor adapters upon storing data in said disk drives.

28. (canceled).

29. (previously presented) The storage system according to claim 21 wherein:

a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters,

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters, and

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter.

30. (previously presented) The storage system according to claim 21 wherein:

said first control information is used to notify said at least one processor adapter of receiving said write request.

31. (currently amended) The storage system according to claim 21 wherein:

said at least one processor adapter detects an area of said memory in which data of said at least one logical volume need to be stored in accordance with said received first control information.

32. (currently amended) The storage system according to claim 21 wherein:

said second control information includes information related to an area of said memory in which data received at each of said first interface adapters need to be stored.

33. (currently amended) The new storage system according to claim 21 wherein:

said at least one processor adapter finds an area of said disk drives related to said at least one logical volume for storing data of said at least one logical volume based on said received first control information.

34. (currently amended) The storage system according to claim 21 wherein:

said third control information includes information related to an area of said disk drives in which data received at each of said second interface adapters need to be stored.

35. (currently amended) The A storage system according to claim 21 wherein:

said at least one processor adapter controls to create a parity data of RAID (Redundant Array of Inexpensive Disks) from data received by at least one of said first interface adapters.

36. (currently amended) A storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume;

[[;]]

a plurality of processor adapters ~~each included at least one processor and~~ controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said at least one logical volume for updating said at least one logical volume, in said at least one disk drive;

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapters and sending data received at said first interface adapter based on a second control information sent from said processor adapters;

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter;

a second interface adapter coupled to said at least one disk drive and receiving data stored in said cache memory adapter from said cache memory adapter based on a third control information sent from said processor adapters asynchronously with receipt of said write request at said first interface adaptor and storing data received at said second interface adapter in said at least one disk drive; and

a switch adapter coupled to said processor adapters, said first interface adapter, said cache memory adapter and said second interface adapter and relaying said data among said first interface adapter, said cache memory adapter and said second interface adapter;

~~wherein said switch adapter relays said first and said second control information between said processor adapters and said first interface adapter and relays said third control information between said processor adapters and said second interface adapter;~~

wherein a~~the~~ number of said processor adapters is~~are~~ increased or decreased, based on a required performance, even though the number of said first interface adapter, said cache memory adapter and said second interface adapter are not increased or decreased, and

wherein each of said processor adapters ~~has~~includes a plurality of ~~micro~~processors and, when a first processing load at said first interface adapter which is coupled to said host computer is greater than a second processing load at

said second interface adapter which is coupled to said at least one disk drive, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter, and

wherein when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adaptereach of said microprocessors is assigned to operate either a first processing load sent from said first interface adapter or a second processing load sent from said second interface adapter in accordance with an amount of the first processing load and an amount of the second processing load.

37. (currently amended) A storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume;

a plurality of processor adapters each including at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said at least one logical volume for updating said at least one logical volume, in said at least one disk drive;

a first interface adapter coupled to said host computer and receiving data sent from said host computer and sending data received at said first interface adapter based on a first control information sent from said processor adapters;

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter;

a second interface adapter coupled to said at least one disk drive and receiving data stored in said cache memory adapter from said cache memory adapter based on a second control information sent from said processor adapters asynchronously with receipt of said data at said first interface adapter and storing said data received at said second interface adapter in said at least one disk drive; and

a switch adapter coupled to said processor adapters, said first interface adapter, said cache memory adapter and said second interface adapter and relaying data of said at least one logical volume among said first interface adapter, said cache memory adapter and said second interface adapter and not relaying data of said at least one logical volume to said processor adapters;

~~wherein said switch adapter relays said first control information between said processor adapters and said first interface adapter and relays said second control information between said processor adapters and said second interface adapter,~~

wherein it is possible to change ~~a~~the number of said processor adapters, independently of the first and second interface adaptors, the cache memory adaptor and the switch adaptor, upon storing data in said at least one disk drive, and based on a required performance, and

wherein each of said processor adapters ~~has~~ includes a plurality of ~~micro~~processors and, when a first processing load at said first interface adapter which is coupled to said host computer is greater than a second processing load at

said second interface adapter which is coupled to said at least one disk drive, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter, and

wherein when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter~~each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapter or a second processing load sent from said second interface adapter in accordance with an amount of the first processing load and an amount of the second processing load~~.

38. (currently amended) A storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume;

a plurality of processor adapters, each ~~including at least one processor and~~ of which controls to store data by determining a location at which the data should be stored, the data being sent from said host computer to said at least one logical volume for updating said at least one logical volume, in said at least one disk drive;

a first interface adapter coupled to said host computer and receiving the data sent from said host computer;

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter;

a second interface adapter coupled to said at least one disk drive, said first interface adapter, said processor adapters, and said cache memory adapter; and

a switch adapter coupled to said processor adapters, said first interface adapter, said cache memory adapter, and said second interface adapter,

wherein said switch adapter relays data between said first interface adapter and said second interface adapter via said cache memory adapter among said first interface adapter, said processor adapters, said cache memory adapter and said second interface adapter based on control information transferred among said first interface adapter, said processor adapters and said second interface adapter of said first interface adapter, said processor adapters, said cache memory adapter, and said second interface adapter, the relaying of the data between said first interface adapter and said second interface adapter being done asynchronously with receipt of the data by the first interface adapter from said host computer,

wherein athe number of said processor adapters isare increased or decreased, independently of the first and second interface adaptors, the cache memory adaptor and the switch adaptor, based on a required performance, and

wherein each of said processor adapters hasincludes a plurality of microprocessors and, when a first processing load at said first interface adapter which is coupled to said host computer is greater than a second processing load at said second interface adapter which is coupled to said at least one disk drive, the number of processors allocated to said first processing load at said first interface

adapter is larger than the number of processors allocated to said second processing load at said second interface adapter, and

wherein when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter~~each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapter or a second processing load sent from said second interface adapter in accordance with an amount of the first processing load and an amount of the second processing load~~.

39. (currently amended) A storage system coupled a host computer, said storage system comprising:

at least one disk drive configuring at least one logical volume;

a plurality of processor adapters ~~including at least one processor and~~ controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said at least one logical volume for updating said at least one logical volume, in said at least one disk drive;

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapters and sending data received at said first interface adapter based on a second control information sent from said processor adapters;

a cache memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter; and

a second interface adapter coupled to said at least one disk drive and receiving data stored in said cache memory adapter from said cache memory adapter based on a third control information sent from said processor adapters asynchronously with receipt of said write request at said first interface adapter and storing data received at said second interface adapter in said at least one disk drive;

wherein said processor adapters are coupled to said first interface adapter and said second interface adapter and send[[sends]] said second control information to said first interface adapter and send[[sends]] said third control information to said second interface adapter,

wherein said first interface adapter sends data to said cache memory adapter among said processor adapters, said cache memory adapter and said second interface adapter,

wherein said second interface adapter receives data from said cache memory adapter among said processor adapters, said cache memory adapter and said first interface adapter, and

wherein said cache memory adapter receives data from said first interface adapter and said second interface adapter among said processor adapters, said first interface adapter and said second interface adapter,

wherein a~~the~~ number of said processor adapters is~~are~~ increased or decreased independently of the first and second interface adaptors and the cache memory adaptor, based on a required performance, and

wherein each of said processor adapters ~~has~~includes a plurality of ~~micro~~processors and, when a first processing load at said first interface adapter which is coupled to said host computer is greater than a second processing load at said second interface adapter which is coupled to said at least one disk drive, the number of processors allocated to said first processing load at said first interface adapter is larger than the number of processors allocated to said second processing load at said second interface adapter,

wherein when said second processing load of said second interface adapter is greater than said first processing load at said first interface adapter, the number of processors allocated to said second processing load of said second interface adapter is larger than the number of said first processing load of said first interface adapter~~each of said microprocessors is assigned to operate either a first processing load sent from said first interface adapter or a second processing load sent from said second interface adapter in accordance with an amount of the first processing load and an amount of the second processing load~~.

40-43. (canceled).

44. (previously presented) The storage system according to claim 21, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

45. (previously presented) The storage system according to claim 36, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

46. (previously presented) The storage system according to claim 37, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

47. (previously presented) The storage system according to claim 38, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

48. (previously presented) The storage system according to claim 39, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

49. (previously presented) The storage system according to claim 40, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

50. (previously presented) The storage system according to claim 41, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

51. (previously presented) The storage system according to claim 42, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

52. (previously presented) The storage system according to claim 43, wherein the cache memory adaptor includes a control information memory module in which information for controlling data transfer are stored.

53. (currently amended) A storage system comprising a first cluster system and a second cluster system,

wherein a first cluster system and a second cluster system each comprises:

a plurality of disk drives;

a plurality of first interface units each coupled to at least one host computer and receiving a write request and data sent from said at least one host computer;

a plurality of second interface units each coupled to said plurality of disk drives and storing the data in said plurality of disk drives asynchronously with the receipt of the write request at the first interface units;

a plurality of processor units separated from said first interface units and said second interface units ~~and each having at least one processor~~;

a cache memory unit having at least one memory, said memory temporarily storing data sent from said first interface units; and

a switch unit coupled to said first interface units, said second interface units[[,]] and said processing units,

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path;

wherein athe number of said processor units of said first cluster system and said second cluster system can be increased or decreased, independently of the first and second interface units, the cache memory unit and the switch unit, based on a required performance, and

wherein each of said processor adapters hasincludes a plurality of microprocessors and, when a first processing load at said first interface adapters which are coupled to said at least one host computer is greater than a second processing load at said second interface adapters which are coupled to said disk drives, the number of processors allocated to said first processing load at said first interface adapters is larger than the number of processors allocated to said second processing load at said second interface adapters, and

wherein when said second processing load of said second interface adapters is greater than said first processing load at said first interface adapters, the number of processors allocated to said second processing load of said second interface adapters is larger than the number of said first processing load of said first interface adapterseach of said microprocessors is assigned to operate either a first processing load sent from said first interface units or a second processing load sent from said second interface units in accordance with an amount of the first processing load and an amount of the second processing load.

54. (previously presented) The storage system according to claim 53,

wherein said processor units in said first cluster system can instruct said plurality of first interface units and the plurality of second interface units of said second cluster system to transfer a data.

55. (new) A storage system according to claim 21,

wherein a plurality of said first interface adapters each receives a read request from at least one host computer, and sends said read request to at least one of said processor adapters, and receives data corresponding to said read request from said cache memory based on a fourth control information sent from said at least one processor adapter.